Exposed Pads: A Brief Introduction

Many of Maxim's recent ICs have "exposed pad" packages. As there have been many questions from our customers on dealing with the exposed pad, this note attempts to provide some general advice.

An exposed pad is an exposed metal plate on an IC package. This application note focuses on pads that are located on the bottom of the package. Exposed pads on the top of the package are less common and their data sheets provide the information the designer needs. For the sake of this application note, consider all pads to be on the bottom, or PCB side of the IC package.

The exposed pad is plated with the same metal or metal alloy as the leads of the IC, usually tin.

Exposed pads are found on many types of packages. Mature package types with gull wing leads, such as TSSOP, offer exposed pads as an optional configuration. On datasheets with TSSOP packages and exposed pads, we are careful to note there is an exposed pad, and the PCB designer must make provisions for its use.

The exposed pad is a standard part of TDFN and QFN packages. They always have exposed pads.

Exposed pads increase the maximum power dissipation of packages. When an exposed pad is offered as an option, it is specifically to increase the power dissipation capabilities of the IC package. (For packages which always have the pad, the pad may or may not be needed for power dissipation. For example, a low-power op amp may see a worst-case power dissipation under 50mW, but be housed in a package capable of safely dissipating over a watt.)

The datasheet for a device with an exposed pad will provide instruction as to the voltage to which the exposed pad should be connected. In most applications, the exposed pad is connected to ground, but be careful to verify this on every device! A blind assumption here can provide a low-impedance short which can take many hours to analyze and a PCB revision to correct.

The pad's dimensions come from the package drawing. Some of Maxim's exposed pad packages have variants with different-sized exposed pads. If the datasheet is not explicit as to which variant is used, contact Maxim/Dallas Applications Tech Support to obtain further information. Create the PCB footprint with information from IPC to ensure proper allowances for

both IC package tolerance and process variance.

In addition to the IPC information, here are some general guidelines for creating the exposed pad's land pattern:

- The pad should be large enough to accommodate the entire exposed pad. This provides a uniform mounting surface as well as a functional keepout area of traces underneath an exposed pad package.
- On ICs which don't need the additional power dissipation of the exposed pad the pad should still be created and connected to the required potential. This eliminates the chance of inadvertently shorting the exposed pad to traces which are routed underneath it.
- On ICs where the exposed pad is intended to provide significant power dissipation, the PCB designer should add vias from the exposed pad's land area to a copper polygon on the other side of the PCB. This provides lower thermal impedance from the IC to the ambient air.
- When creating the solder paste screen, an opening should be created for the exposed pad. This way the exposed pad will be electrically and thermally connected to the PCB.
- If the board must be hand assembled, a small amount of electrically conductive adhesive can be used, but this makes rework of the PCB virtually impossible. Another alternative to facilitate hand assembly is to include a single large via in the center of the land to allow the application of a soldering iron to the bottom of the IC through this hole. This is a compromise, and should only be used when necessary. The best approach is to use a standard SMT assembly process with carefully controlled parameters to ensure reliable and repeatable results.